Listing of Claims

1. (Currently Amended) A circuit arrangement for controlling a display device which can be operated in a partial mode, the circuit arrangement comprising:

a row drive circuit for driving n rows of the display device sequentially from 1 to n, the row drive circuit responsive to a row enable signal that is provided to each row from 1 to n; and

a column drive circuit for driving m columns of the display device~~, wherein the row drive circuit controls the n rows of the display device sequentially from 1 to n, and the column drive circuit~~ by supplying[[ies]] column voltages to the m columns, the column voltages corresponding to picture data to be displayed [[of]] as pixels of the controlled row, characterized in that a logic function is included in the row drive circuit in front of at least one row output, ~~to which~~ the logic function configured and arranged to respond to a first control signal, indicative of whether or not the partial mode is to be implemented, ~~is supplied, said first control signal achieving a deactivation/activation of~~ by preventing the at least one row output from driving the row in response to the row enable signal ~~in dependence on the partial mode~~.

2. (Previously presented) A circuit arrangement as claimed in claim 1, characterized in that the logic function is connected in front of each row output.

3. (Previously presented) A circuit arrangement as claimed in claim 1, characterized in that the logic function is realized as an AND gate.

4. (Previously presented) A circuit arrangement as claimed in claim 1, characterized in that the row drive circuit comprises a shift register which has n stages and n outputs, and in that a second control signal can be supplied to the shift register at an input thereof for controlling the consecutive rows 1 to n, which second control signal activates the outputs of the shift register consecutively in dependence on a clock signal.

5. (Previously presented) A circuit arrangement as claimed in claim 2, characterized in that the first control signal is capable of switching off all n row outputs by means of the logic function during control of a line that is not to be displayed in the partial mode.

6. (Previously presented) A circuit arrangement as claimed in claim 1, characterized in that control logic in the column drive circuit generates the first control signal in dependence on the partial mode and supplies the first control signal to the row drive circuit.

7. (Previously presented) A circuit arrangement as claimed in claim 1, characterized in that the column drive circuit supplies no column voltages to the m columns in a case of a line that is not to be displayed.

8. (Previously presented) A circuit arrangement as claimed in claim 4, characterized in that the frequency of the clock signal can be increased in a case of one or several consecutive rows that is or are not to be displayed.

9. (Previously presented) A row drive circuit for controlling n rows of a display device that is operable in a partial mode, the row drive circuit having n outputs, with a logic function connected in front of each of the row outputs, wherein the logic function deactivates/activates the row outputs in dependence on the partial mode responsive to a first control signal.

10. (Previously presented) A display device comprising a circuit arrangement as claimed in claim 1.

11. (Previously presented) An electronic appliance comprising a display device as claimed in claim 10.

12. (Currently Amended) A method of realizing a partial mode of a display device, the display device controlled by a circuit arrangement that includes a row drive circuit

for driving n rows and a column drive circuit for supplying column voltages to m columns, the method comprising:

sequentially providing an enable signal to each row ~~controlling the n rows~~ from 1 to n;

supplying the column voltages to the m columns for displaying corresponding picture data,

deactivating all row outputs of a first row of the row drive circuit in response to a first control signal ~~when~~ indicating that the first [[a]] row is not to be displayed in the partial mode of the display device, and

activating all ~~of the~~ row outputs of a second row, in response to the enable signal and the first control signal ~~when~~ indicating that the [[a]] row is to be displayed in the partial mode.

13. (Previously presented) A circuit arrangement as claimed in claim 4, wherein each of the stages includes a flipflop.

14. (Previously presented) A circuit arrangement as claimed in claim 4, wherein the first control signal overrides the second control signal.